POWER MOSFET DATA BOOK

#D11

August, 1985

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DIPLOMAT ELECTRONICS CORPORATION
20151 Bahama Street
Chatsworth, California 91311
(213) 644-7596
(818) 700-8700 (818) 341-4411

INTRODUCTION

In 1977, HITACHI was the first in the world to develop and mass-produce 100 Watt Complementary Power MOS FETs. Since then, Power MOS FETs have been used in a variety of fields as an ideal power device with high switching speed and high resistance to electrically induced failure. HITACHI Power MOS FET technology has consistently advanced in the areas of on-resistance, voltage and current handling capability and packaging.

POWER MOS FET FEATURES:

A. Excellent frequency response and high switching speed. (No carrier storage effects.)
B. High resistance to electrical destruction. (No current concentration effects.)
C. Easy parallel connection for higher power applications.
D. Minimum drive power. (Voltage controlled device.)

There are two basic Power MOS FET structures: Vertical Type and Lateral Type. The advantages of Vertical Types are: a) Drain Case and b) low on-resistance and low loss. Advantages of Lateral Types are: a) Source Case, b) high resistance to electrical destruciton, and c) high frequency response. HITACHI has both types to meet various requirements. The Vertical Types are called "D Series", and the Lateral Types are called "S Series".

Power MOS FETs show extreme advantages, not only in new fields where conventional power devices are inadequate, but also in existing fields where conventional devices are already in use.

STRUCTURE & FEATURES

Hitachi has two types of Power MOS FETs, D Series (vertical structure) and S Series (lateral structure), as shown in Fig. 2-1 and Fig. 2-2. Although there are some differences in their characteristics, both have the following advantages.

- Good frequency response and high switching speed due to absence of carrier storage effect.
- Free from current concentration, and hence have high resistance to destruction.
- Require a very low driving power as they are voltage controlled devices.

To understand the structure and features of Power MOS FETs, we would like to show the N-channel MOS FET.

Fig. 2-3 shows the N-channel MOS FET structure. This is called an MOS structure, because the current control gate region is made of three layers, Metal, Oxide and Silicon. The charged particles (electrons, here) are produced from Source and flow to and out of Drain.

When a positive voltage is applied to the gate electrode, in proportion to it, a depletion layer will be produced on the silicon surface beneath the gate. Then negative charges (electrons) will appear on it, which cause the silicon surface to be inverted from P type substrate to N type layer. This inverted layer is channel.

When a voltage is applied between Drain and

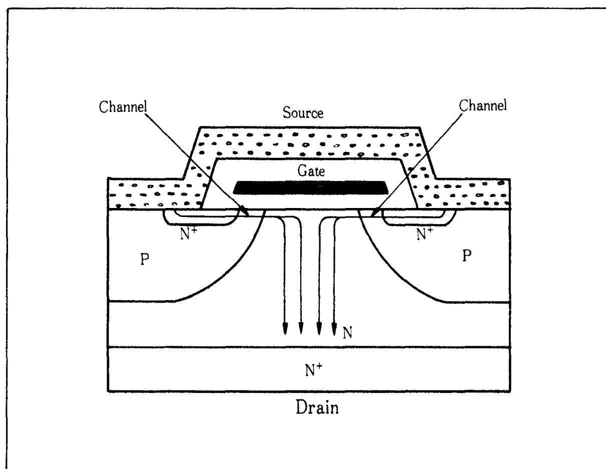


Fig. 2-1 Structure of D series (Vertical type) (N channel)

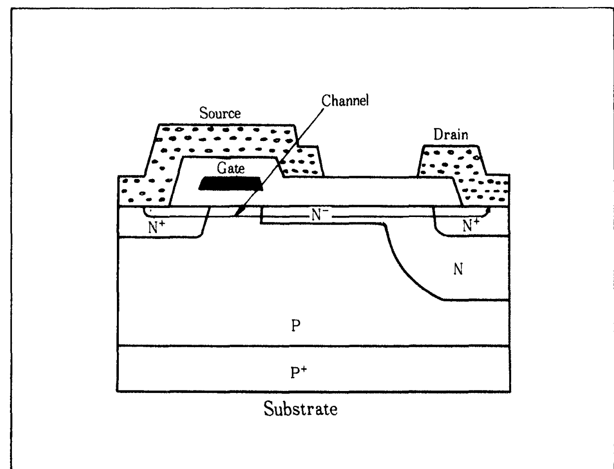


Fig. 2-2 Structure of S series (Lateral type) (N channel)

Source, electrons in the channel will move to the Drain, which means that the drain current flows.

There are two types of FETs, depletion type (normally ON type) and enhancement type (normally OFF type). In the case of depletion type FETs, drain current flows even if the gate voltage is 0V, in contrast to enhancement type FETs. Hitachi Power MOS FETs are all enhancement type (normally OFF type).

The gate voltage at which the drain current begins to flow is gate cut-off voltage V_{GS} (off). (Fig. 2-4).

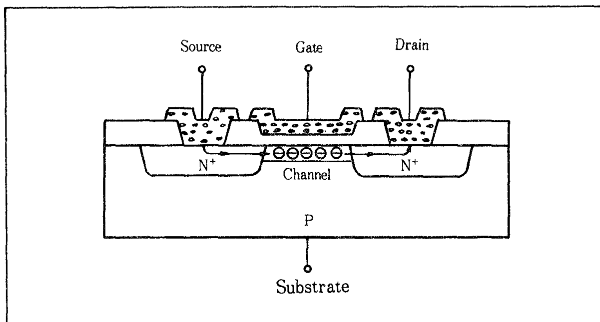


Fig. 2-3 Basic Structure of MOS FET (Lateral type)

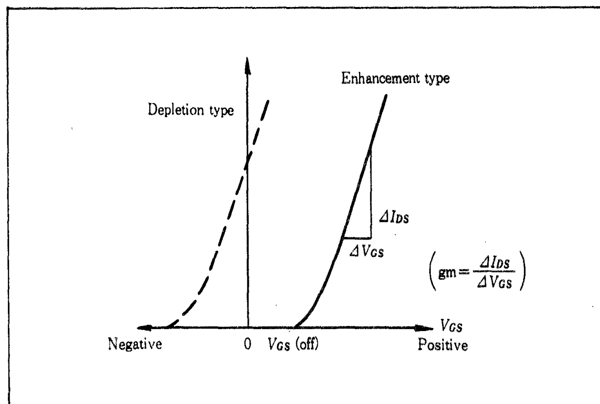


Fig. 2-4 Transfer Characteristics

Normally, there is a quadratic correlation between I_{DS} and V_{GS}. The slope of its curve gives the mutual conductance g_m $(=\frac{\Delta I_{DS}}{\Delta V_{GS}})$, that shows amplification factor.

Breakdown voltage of the drain varies with the structure between the N^+ region of the drain and the gate electrode, as shown in Fig. 2-3. There is only a thin oxide film between the N^+ region and the gate electrode, so the field gradient will be high. This makes it difficult to achieve high drain to gate breakdown voltage, limited to 20 ~ 30V in typical MOS FETs.

By widening the space between the N^+ region of the drain and the gate electrode, and easing the electric field concentration, we can make the breakdown voltage larger.

There are two fabrication methods used to make the breakdown voltage higher, one is D series (vertical structure) and the other is S series (lateral structure). We would like to further explain about their structures and features, with Fig. 2-1 and Fig. 2-2.

● D Series (vertical structure)

In D series the drain (N^+) is placed beneath the silicon substrate. The gate electrode covers over the N region between P channels, to ease the electric field concentration beneath the gate. The electrons flow out of the source and reach to the N region through the P channels horizontally. On the surface of the N region, there is an accumulation layer of N^+ produced by the positive voltage applied to the gate electrode. Therefore, the electrons are attracted to the accumulation layer, to flow to the drain through the N region vertically.

Consequently, the D series is referred to as a vertical structure. In this structure, the case is connected to the drain.

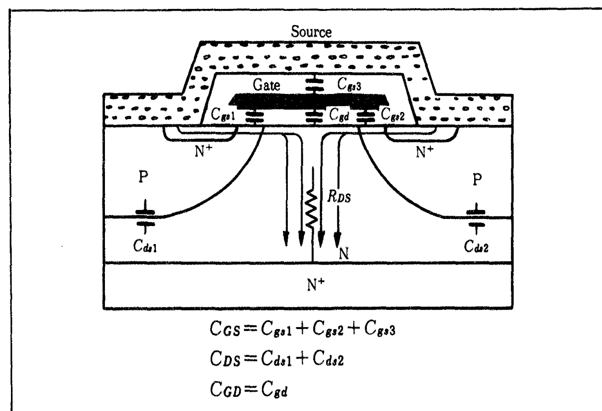


Fig. 2-5 Structure of D series (Vertical type) (N channel)

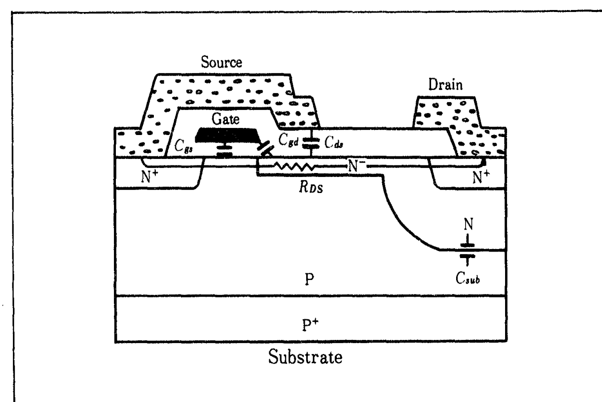


Fig. 2-6 Structure of S series (Lateral type) (N channel)

In the D series the channel (N region) is placed in the silicon, and the size of one unit can

be smaller than that of S series. This enables the switching ON resistance of D series to be smaller than that of S series with the same voltage and the same chip size.

Electrostatic capacitances are the junction capacitances and the MOS capacitances as shown in Fig. 2-5.

Here, the capacitance between the drain and the gate, C_{GD}, is relatively large, so in the source earth circuit, C_{GD}'s effects to the input capacitance (C_{iss}), to the output capacitance (C_{oss}) and to the feedback capacitance (C_{rss}) should be considered.

The gate electrode is made of polysilicon, which has long been used effectively in CMOS LSI. Polysilicon resistance is about 100 times larger than that of metals. When using it for the gate electrode, we lower the gate resistance by using a mesh gate pattern, and by connecting the polysilicon gate and the metal electrode effectively. To find the switching time of the vertical structure, more complicated operation analysis is required, because the feed back capacitance (C_{gd}) is large and the voltage dependence of the drain resistance is large. The input capacitance can't be determined simply by the time constant of the gate resistance. This will be further explained in the switching characteristics, paragraph 5.3.

● **S Series (lateral structure)**

In S series, the drain (N^+ region) is placed on the surface of the silicon. The region between the drain (N^+) and P channel is an N region produced by ion implantation, and it makes the strength of the electrostatic field even. Moreover, the source electrode is extended to cover a part of the N region, working as a field plate to prevent electrostatic field concentration around the gate. The electrons flow out of the source and reach to the drain through the P channel and the N region laterally. This is why the S series is called a lateral structure.

The substrate is connected to the source electrode, and the case to the source.

The feed back capacitance (C_{rss}) is indicated as C_{gd} in Fig. 2-6. The source field plate is extended above the N region, so the C_{gd} is shielded by the field plate and the capacitance of the N region (C_{ds}). This results in a very small value of feed back capacitance (C_{rss}).

From the view points of chip and package, the S series is very suitable for high frequency use, because the input and the output leads are separated electrically. Like in the D series, we usually use polysilicon for the gate electrode. Moreover, we can provide devices with metal gates for very high speed. In the polysilicon gate FET, the frequency limit is determined by the time constant of the input capacitance and the gate resistance. In the metal gate FET, it is determined by the lead inductances of the gate and the source, because the gate resistance is very small.

Table 2-1 shows the small signal equivalent circuit and the vertical characteristics of D series and S series.

Table 2-1 Equivalent Circuits and Features, Parameters

Item \ Structure		Off-set Gate Type	Vertical Type
Equivalent Circuit		S, G, D, R_g, C_{GS}, C_{GD}, R_{ON}, C_{DS}	C_{GD}, R_{ON}, R_g, C_{DS}, C_{GS}; S, G, C_{GS}, R_g, C_{GD}, C_{DS}, R_{ON}, D
Features	R_g	Large (22Ω)*, However, it is able to be decreased by 2 figures with Metal-gate	Small (2.5Ω)*
	C_{iss}	Small (800pF)**	Large (1800pF)**, C_{GD} is increased enormously at low Drain Voltage
	C_{oss}	Large (350pF)**	Small (190pF)**
	C_{rss}	Small (15pF)**, Slightly depend on Drain Voltage	Large (85pF)**, C_{GD} heavily depends on Drain Voltage
	R_{ON}	Large (2.2Ω)*	Small (1Ω)*
	g_m	Small (1.0S)*	Large (1.8S)*
	ASO	Good	Fair

(Note) *Typical value of V_{DSS}=400V, I_D=5A rating. **Test Condition: V_{DS}=10V, V_{GS}=−5V, f=1MHz

CHARACTERISTICS OF POWER MOS FETS

5.1 Output Characteristics

Fig. 5-1 shows the output characteristics of the D series 2SK413 and S series 2SK134, which have the same specification. Whereas in a small signal MOS FET the forward transconductance $|Y_{fs}|$ is 10 ~ 20 mS (milli-Siemens) at best, in a power MOS FET it is 1.0 ~ 15S. Also, as is obvious from Fig. 5-1, they have what is called pentode characteristics and excellent linearity of $|Y_{fs}|$ in relation to I_D.

P channel MOS FETs also have similar characteristics. P channel and N channel types have complementary characteristics.

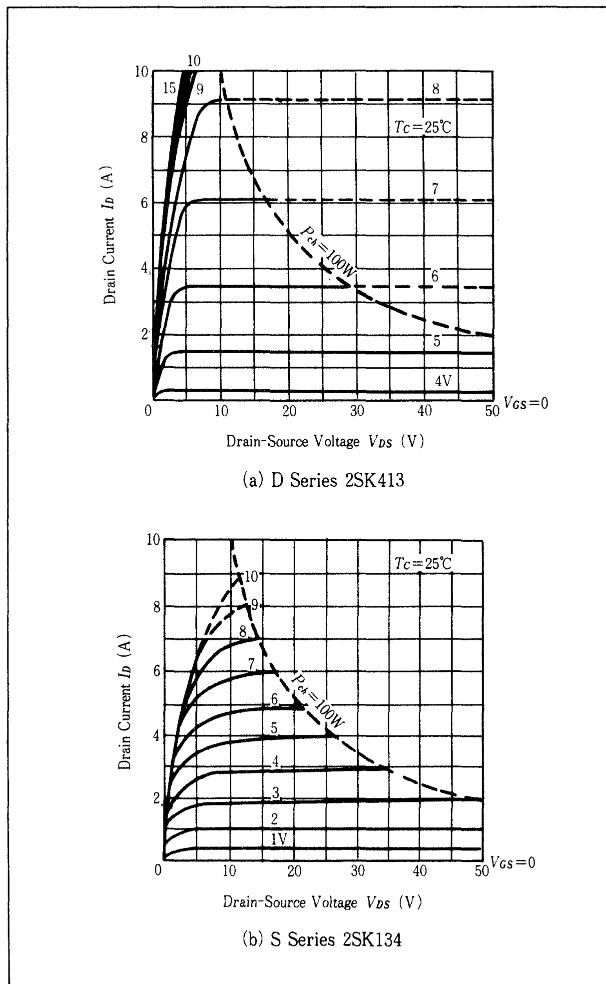


Fig. 5-1 Typical Output Characteristics

5.2 Frequency Response Characteristics

One of the outstanding features of the power MOS FET is that it has excellent high speed and high frequency characteristics. Therefore, they can be applied in high-speed switching regulators, high-output broadcasting transmitters, etc.

The cut-off frequency of an intrinsic MOS FET is defined by the ratio of the mutual conductance and the input capacitance, and in a typical MOS FET, it will be in the order of GHz. In fact, however, the cut-off frequency is limited by the parasitic resistance and the input capacitance of the gate.

Fig. 5-2 shows the equivalent circuit of MOS FET in the saturation region.

In Fig. 5-2, the cut-off frequency (f_c), at which the voltage gain falls to −3dB of its low-frequency value, is given by the following equation.

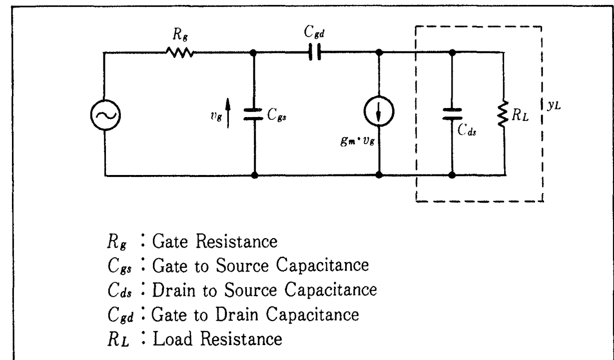


Fig. 5-2 Equivalent circuit of MOS FET

$$f_c \simeq \frac{1}{2\pi} \cdot \frac{1}{R_g\{C_{gs} + (1 - A_0)C_{gd}\}} \quad \cdots\cdots (1)$$

Here, A_0 is the low-frequency voltage gain, and R_g is the series resistance of the gate.

Fig. 5-3 shows the cut-off frequencies of the vertical and the lateral structure devices, found by substituting into equation (1) the parameters (calculated values) of a power MOS FET which has a silicon gate. In the lateral structure, C_{gd} is much smaller than C_{gs}, and can be neglected.

In the vertical structure, as explained in paragraph 2, C_{gs} is a function of the voltage gain (A_0) in the low frequency region, because C_{gd} is large.

We would like to summarize the above, as follows.

(1) In the case of low voltage gain, the cut-off frequencies of the vertical and the lateral structures show the same level. The input impedance ratio at f_C depends on R_g ratio, so the impedance of the vertical structure is 1.5 ~ 2 times lower than that of the lateral structure.

(2) In the case of high gain amplifier circuits, the frequency characteristics of the lateral structure and better than that of the vertical structure, because in the vertical structure the feedback capacitance (C_{gd}) has a great influence.

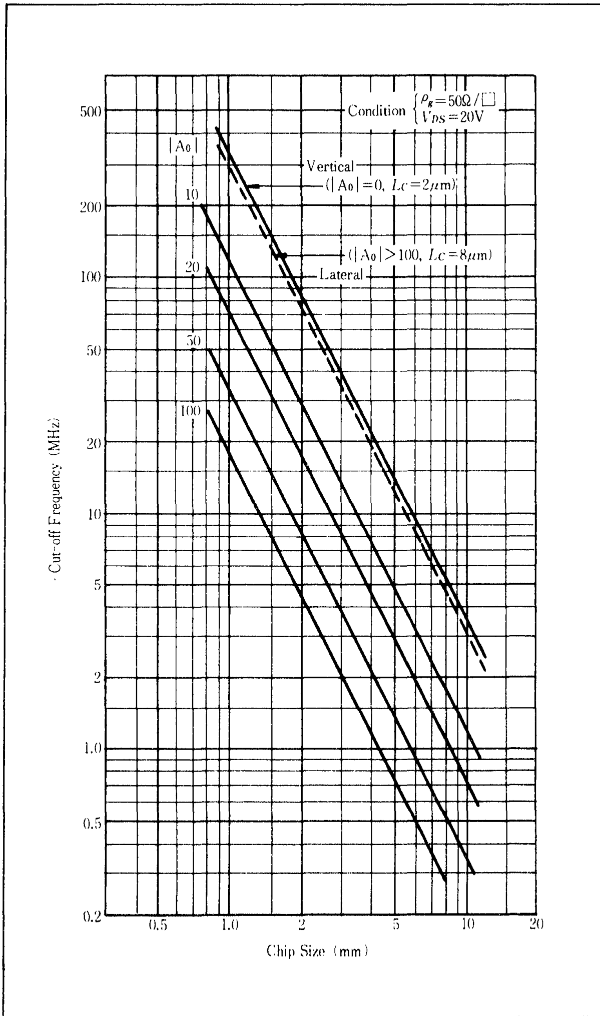


Fig. 5-3 Cut-off Frequency of Silicon Gate Power MOS FETs

To further improve the frequency characteristics, the use of low resistance material such as metal is required. This will improve the cut-off frequency by 10 ~ 100 times. Fig. 5-4 shows the frequency characteristics and the test circuits of typical kinds of MOS FETs. In 2SK317 and 2SK221Ⓗ, the gate material is metal-gate.

5.3 Switching Characteristics

When using power MOS FETs for power switching, such as in switching regulators, the

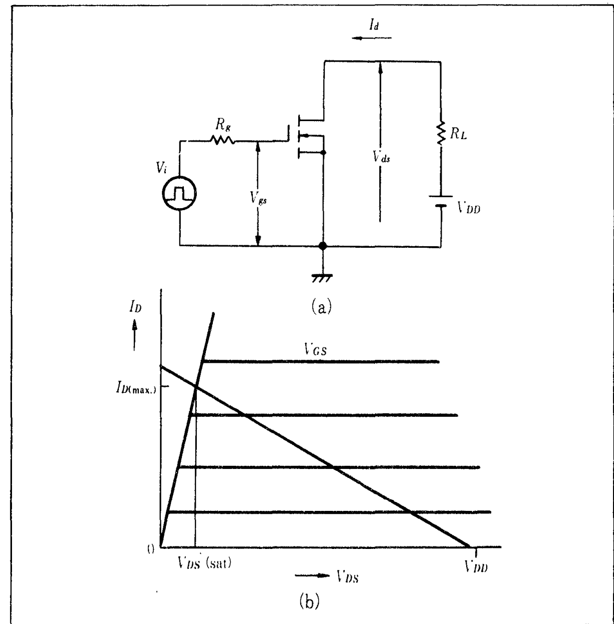


Fig. 5-5 Switching Circuit and Typical Output Characteristics & Load Curve

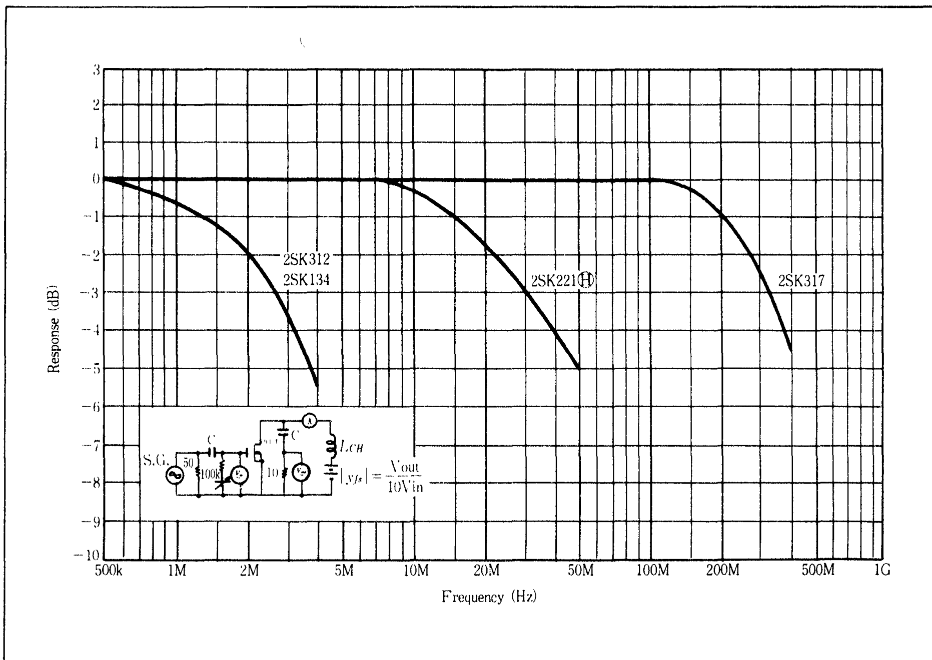


Fig. 5-4 Frequency Response Characteristics of y_{fs} (Source Common)

load of the switching device is usually inductive. Here, however, we would like to assume a resistance load, because it can be treated easily.

Fig. 5-5 shows the resistance load switching circuit (a), simplified current-voltage characteristics, and the load line (b). In this figure, we suppose that the rising curve of current vs. voltage is shown by a straight line, and g_m=0.

Therefore, in Fig. 5-5 (b), the point of the drain voltage=V_{DS}

result, characteristics worsen, as high frequency gain drops and phase shift increases.

This is expressed in Fig. 5-42. The equivalent circuit with passive devices alone is represented in Fig. 5-43.

It has been verified experimentally that the phase differential of V_{O1} and V_{O2} can be eliminated and driving in the same phase can be achieved by equalizing C_g with C_{in2} and that phase shift as 100 kHz can be limited within −90 degrees.

5.9 Analysis of Oscillation in Source Follower Circuits

<Reference>

There have been many works on analysis of oscillation in source follower circuits. The most general analysis for source follower circuits is about the case in which the real part of the input impedance is negative and the imaginary part is ZERO. An example is described as followers. The sumplified equivalent circuit of source follower is shown in Fig. 5-44.

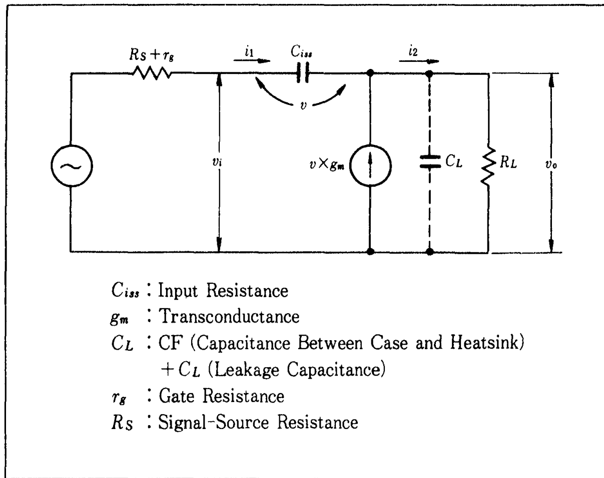


Fig. 5-44 Equivalent Circuit of Source Follower Circuit

The input impedance Z_{in} can be obtained as follows;

$$Z_{in} = \frac{v_i}{i_1} = \frac{1}{j\omega C_{iss}} + R_L\left(1 + \frac{g_m}{j\omega C_{iss}}\right) \quad \ldots\ldots (1)$$

In the case of load consisting of paralleled resistor and capacitor Substitute $\frac{R_L}{1+j\omega C_L R_L}$ instead of R_L in equation (1).

$$Z_{in} = \frac{1}{j\omega C_{iss}} - \frac{j\omega C_L R_L^2}{1+\omega^2 C_L^2 R_L^2} - \frac{j\omega g_m R_L}{(1+\omega^2 C_L^2 R_L^2)\omega^2 C_{iss}} + \frac{R_L}{1+\omega^2 C_L^2 R_L^2} - \frac{\omega^2 C_L R_L^2 g_m}{(1+\omega^2 C_L^2 R_L^2)\omega^2 C_{iss}} \quad \ldots (2)$$

The condition for negative resistance is;

$$R_s + r_g + \frac{R_L}{1+\omega^2 C_L^2 R_L^2} - \frac{C_L R_L^2 g_m}{(1+\omega^2 C_L^2 R_L^2) C_{iss}} < 0 \quad \ldots\ldots\ldots\ldots (3)$$

moreover, approximately,

$$R_s + r_g + R_L - \frac{C_L R_L^2 g_m}{C_{iss}} < 0 \quad \ldots\ldots\ldots (4)$$

Therefore, to prevent oscillation, external gate resistor R_G should be inserted. Then the following equation can be obtained.

$$R_G + R_s + r_g + R_L - \frac{C_L R_L^2 g_m}{C_{iss}} \geqq 0$$

However, the insertion of external R_G makes Power MOS FETs frequency response worse. Therefore, when selecting R_G, a compromise between stability against oscillation and amplifier's frequency response should be considered. Voltage gain vs. frequency vs. R_G is shown in Fig. 5-45.

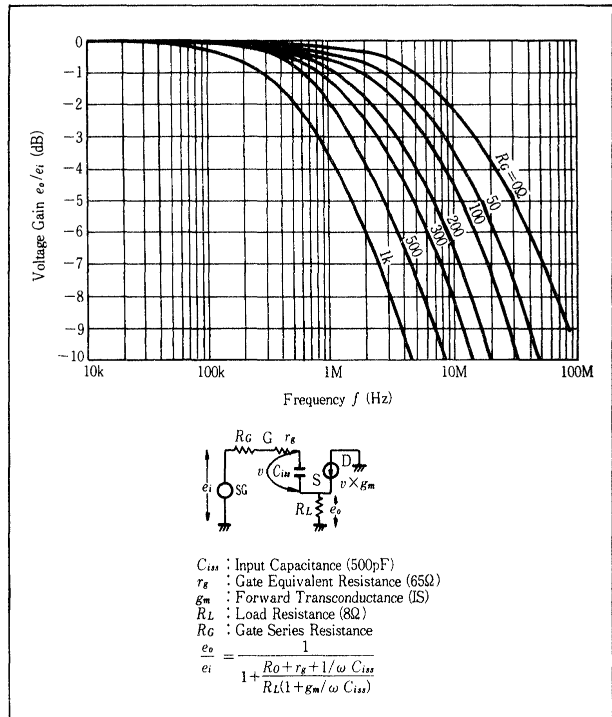


Fig. 5-45 Frequency Characteristics of Source Follower (Calculated Value)

2SJ48,2SJ49,2SJ50

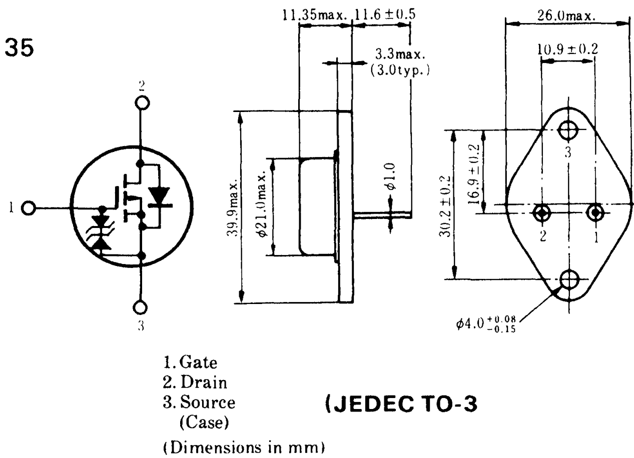
SILICON P-CHANNEL MOS FET

LOW FREQUENCY POWER AMPLIFIER

Complementary Pair with 2SK133, 2SK134, 2SK135

■ FEATURES

- High Power Gain.
- Excellent Frequency Response.
- High Speed Switching.
- Wide Area of Safe Operation.
- Enhancement-Mode.
- Good Complementary Characteristics.
- Equipped with Gate Protection Diodes.



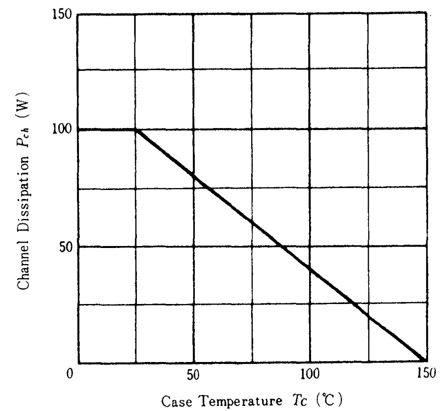
(JEDEC TO-3

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating			Unit
		2SJ48	2SJ49	2SJ50	
Drain-Source Voltage	V_{DSX}	−120	−140	−160	V
Gate-Source Voltage	V_{GSS}	±14			V
Drain Current	I_D	−7			A
Body-Drain Diode Reverse Drain Current	I_{DR}	−7			A
Channel Dissipation	P_{ch}*	100			W
Channel Temperature	T_{ch}	150			°C
Storage Temperature	T_{stg}	−55 ~ +150			°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

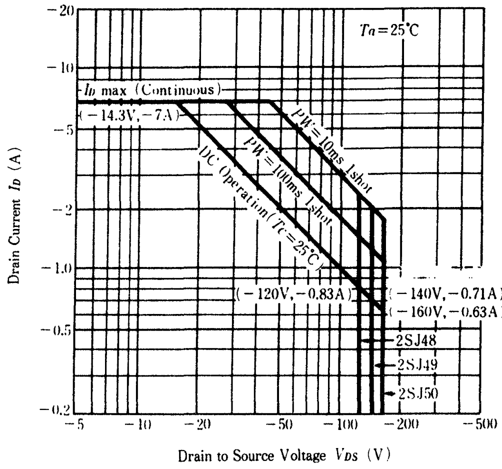


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

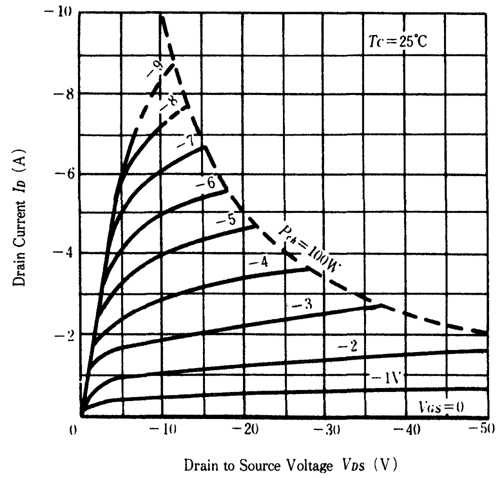
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SJ48	$V_{(BR)DSX}$	I_D=−10mA, V_{GS}=10V	−120	—	—	V
	2SJ49			−140	—	—	V
	2SJ50			−160	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±14	—	—	V
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=−100mA, V_{DS}=−10V	−0.15	—	−1.45	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=−7A, V_{GD}=0*	—	—	−12	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=−3A, V_{DS}=−10V*	0.7	1.0	1.4	S
Input Capacitance		C_{iss}	V_{GS}=5V, V_{DS}=−10V, f=1MHz	—	900	—	pF
Output Capacitance		C_{oss}		—	400	—	pF
Reverse Transfer Admittance		C_{rss}		—	40	—	pF
Turn-on Time		t_{on}	V_{DD}=−20V, I_D=−4A	—	230	—	ns
Turn-off Time		t_{off}		—	110	—	ns

*Pulse Test

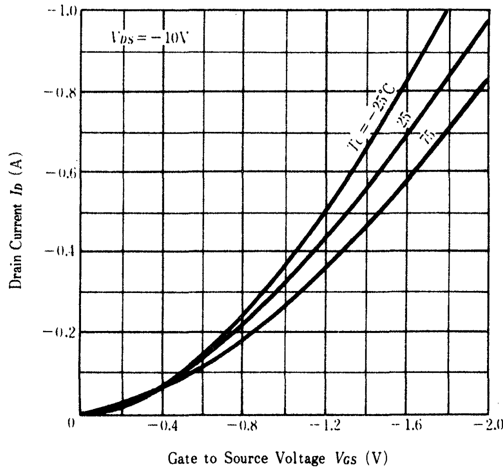
MAXIMUM SAFE OPERATION AREA



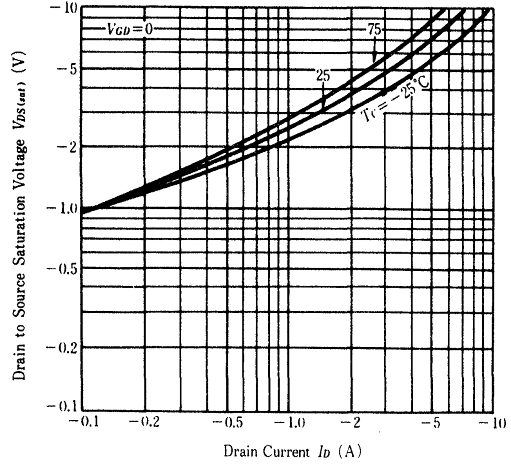
TYPICAL OUTPUT CHARACTERISTICS



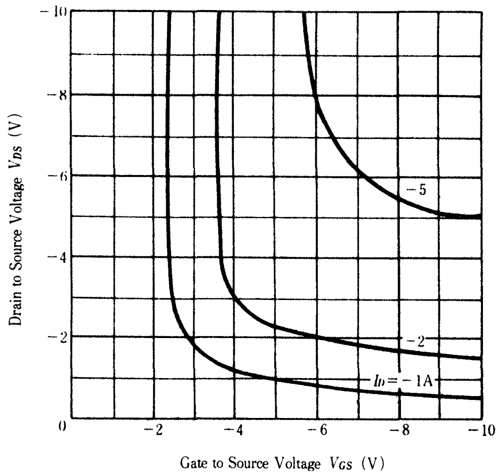
TYPICAL TRANSFER CHARACTERISTICS



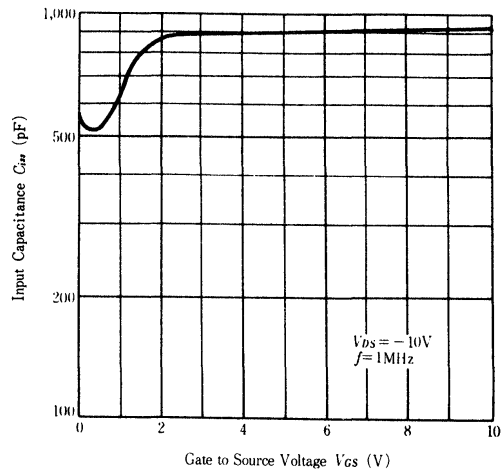
DRAIN TO SOURCE SATURATION VOLTAGE VS. DRAIN CURRENT



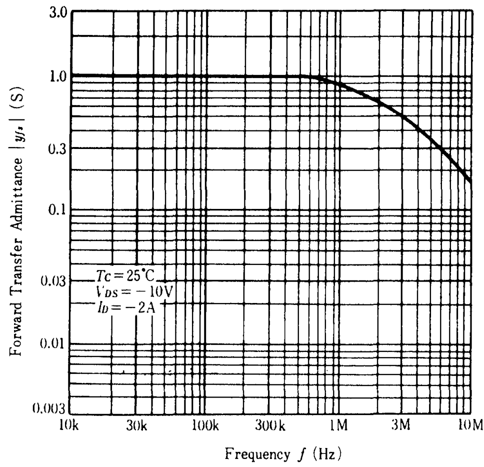
DRAIN TO SOURCE VOLTAGE VS. GATE TO SOURCE VOLTAGE



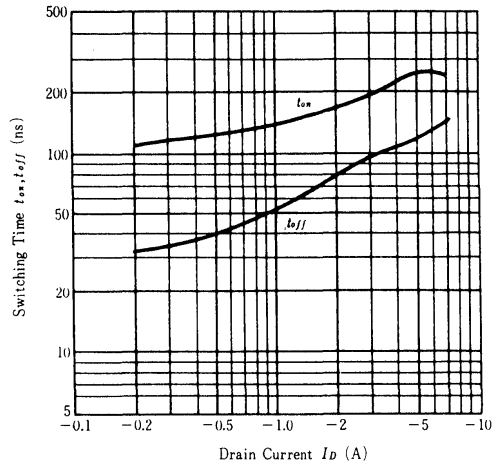
INPUT CAPACITANCE VS. GATE TO SOURCE VOLTAGE



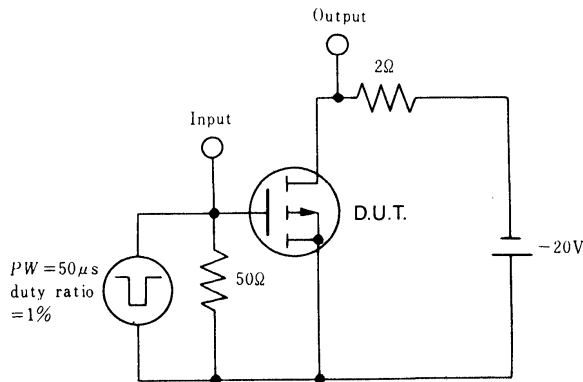
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



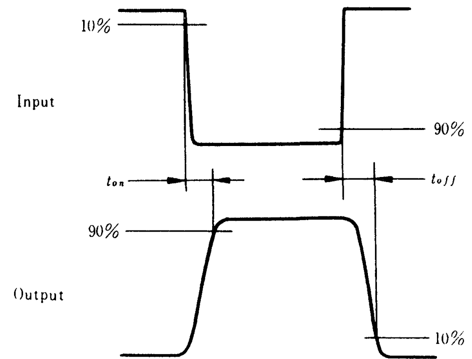
SWITCHING TIME VS. DRAIN CURRENT



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



2SJ55, 2SJ56

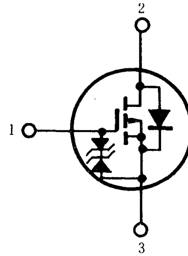
SILICON P-CHANNEL MOS FET

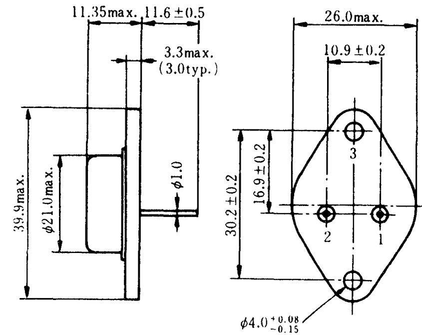
LOW FREQUENCY POWER AMPLIFIER

Complementary Pair with 2SK175, 2SK176

■ FEATURES

- High Power Gain.
- Excellent Frequency Response.
- High Speed Switching.
- Wide Area of Safe Operation.
- Enhancement-Mode.
- Good Complementary Characteristics.
- Equipped with Gate Protection Diodes.





(JEDEC TO-3)

1. Gate
2. Drain
3. Source (Case)

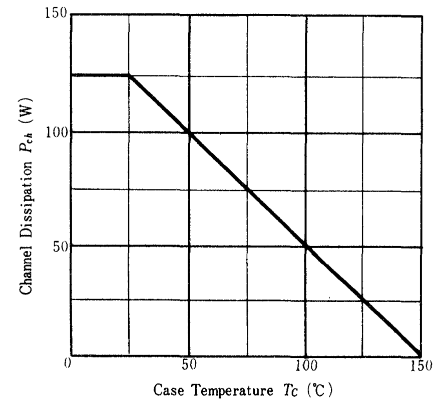
(Dimensions in mm)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SJ55	2SJ56	
Drain-Source Voltage	V_{DSX}	−180	−200	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	−8		A
Body-Drain Diode Reverse Drain Current	I_{DR}	−8		A
Channel Dissipation	P_{ch}*	125		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

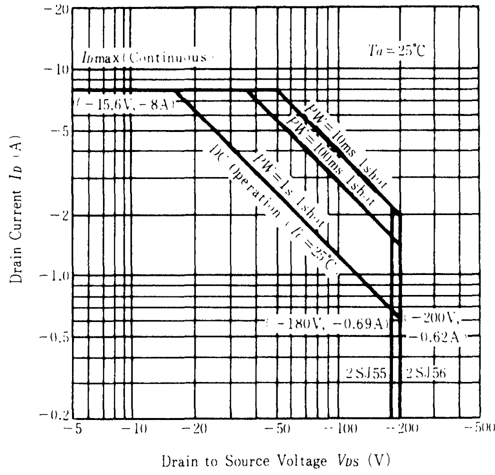


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

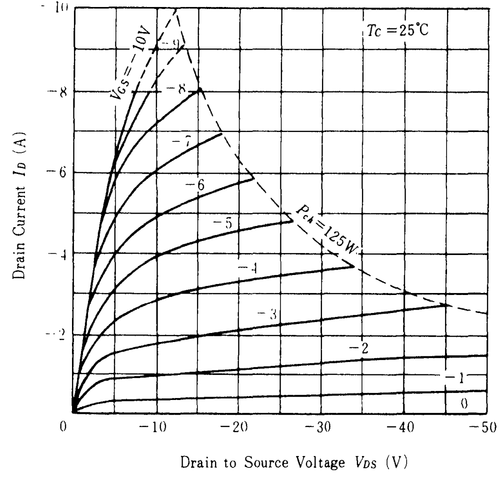
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SJ55	$V_{(BR)DSX}$	I_D=−10mA, V_{GS}=10V	−180	—	—	V
	2SJ56			−200	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=−100mA, V_{DS}=−10V	−0.15	—	−1.45	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=−8A, V_{GD}=0*	—	—	−12	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=−3A, V_{DS}=−10V*	0.7	1.0	1.4	S
Input Capacitance		C_{iss}	V_{GS}=5V, V_{DS}=−10V, f=1MHz	—	1200	—	pF
Output Capacitance		C_{oss}		—	700	—	pF
Reverse Transfer Capacitance		C_{rss}		—	60	—	pF
Turn-on Time		t_{on}	V_{DD}=−30V, I_D=−4A	—	320	—	ns
Turn-off Time		t_{off}		—	120	—	ns

*Pulse Test

MAXIMUM SAFE OPERATION AREA



TYPICAL OUTPUT CHARACTERISTICS



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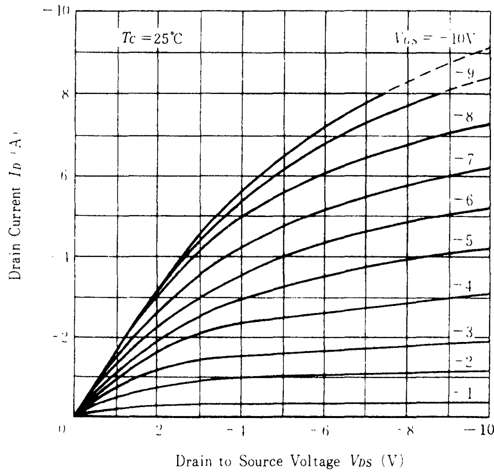

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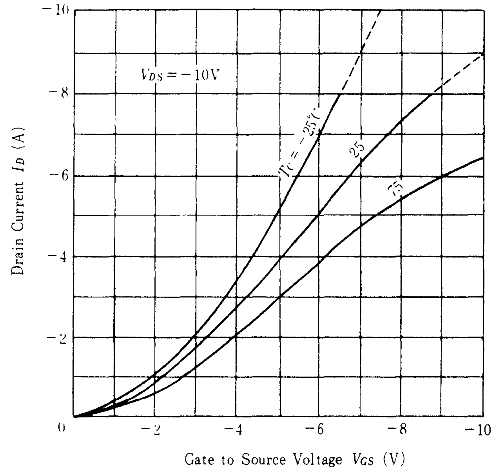
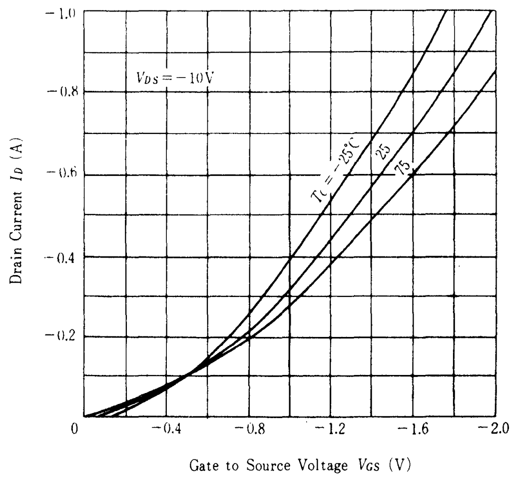
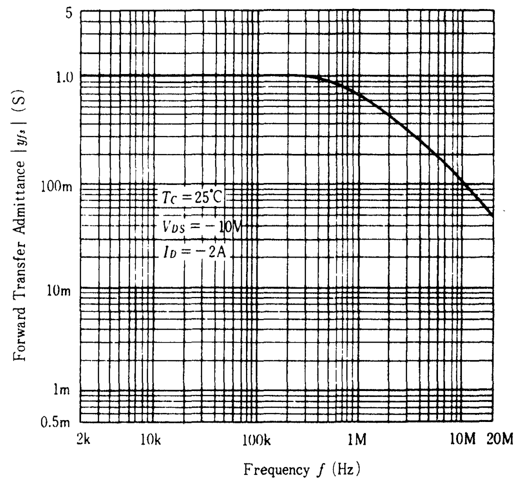


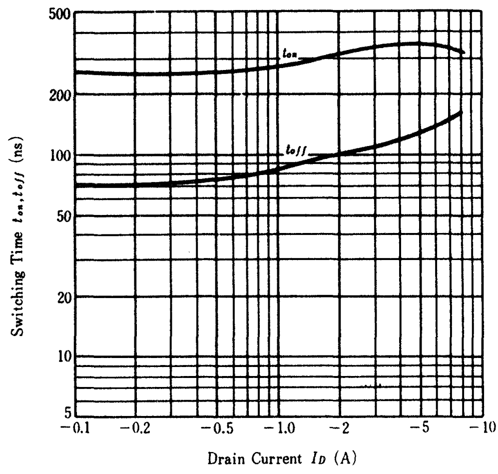
TYPICAL TRANSFER CHARACTERISTICS



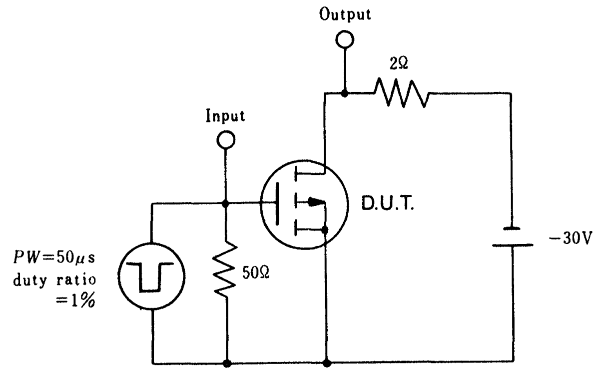
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



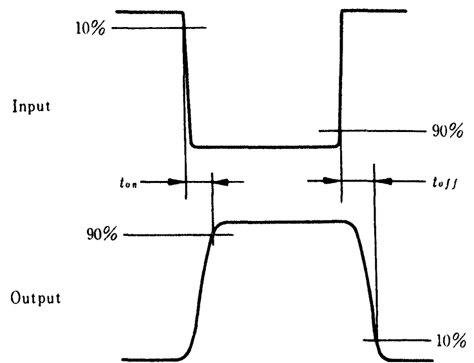
SWITCHING TIME VS. DRAIN CURRENT



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



2SK133, 2SK134, 2SK135

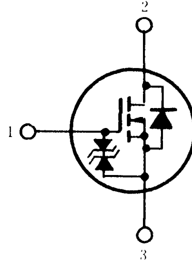
SILICON N-CHANNEL MOS FET

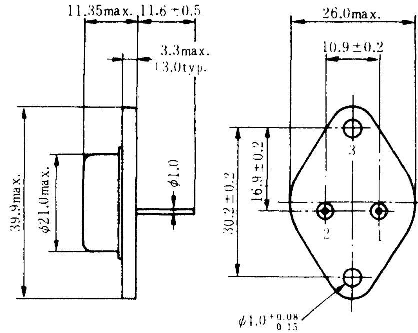
LOW FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ48, 2SJ49, 2SJ50

■ FEATURES

- High Power Gain.
- Excellent Frequency Response.
- High Speed Switching.
- Wide Area of Safe Operation.
- Enhancement-Mode.
- Good Complementary Characteristics.
- Equipped with Gate Protection Diodes.





1. Gate
2. Drain
3. Source
(Case)
(Dimensions in mm)

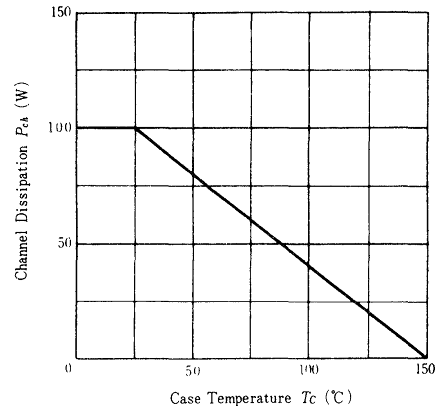
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating			Unit
		2SK133	2SK134	2SK135	
Drain-Source Voltage	V_{DSX}	120	140	160	V
Gate-Source Voltage	V_{GSS}	±14			V
Drain Current	I_D	7			A
Body-Drain Diode Reverse Drain Current	I_{DR}	7			A
Channel Dissipation	P_{ch}*	100			W
Channel Temperature	T_{ch}	150			°C
Storage Temperature	T_{stg}	−55 ~ +150			°C

*Value at T_c=25 °C

POWER VS. TEMPERATURE DERATING

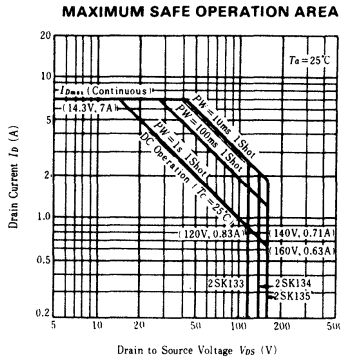


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

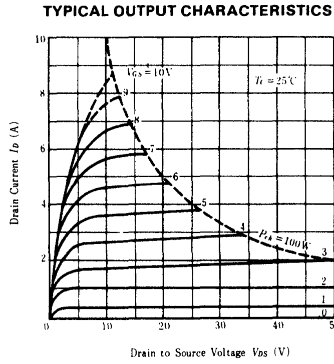
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK133	$V_{(BR)DSX}$	I_D=10mA, V_{GS}=−10V	120	—	—	V
	2SK134			140	—	—	V
	2SK135			160	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±14	—	—	V
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=100mA, V_{DS}=10V	0.15	—	1.45	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=7A, V_{GD}=0*	—	—	12	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	0.7	1.0	1.4	S
Input Capacitance		C_{iss}	V_{GS}=−5V, V_{DS}=10V, f=1MHz	—	600	—	pF
Output Capacitance		C_{oss}		—	350	—	pF
Reverse Transfer Capacitance		C_{rss}		—	10	—	pF
Turn-on Time		t_{on}	V_{DD}=20V, I_D=4A	—	180	—	ns
Turn-off Time		t_{off}		—	60	—	ns

*Pulse Test

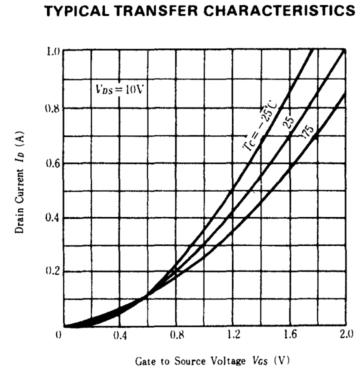
MAXIMUM SAFE OPERATION AREA



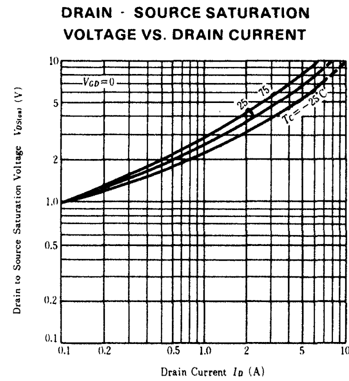
TYPICAL OUTPUT CHARACTERISTICS



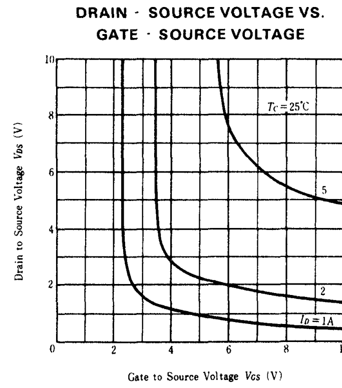
TYPICAL TRANSFER CHARACTERISTICS



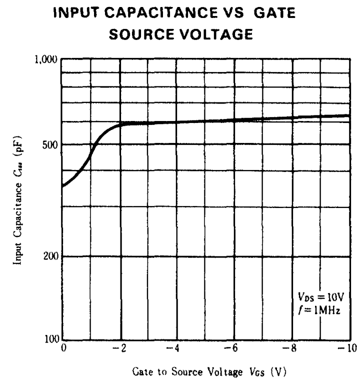
DRAIN - SOURCE SATURATION VOLTAGE VS. DRAIN CURRENT



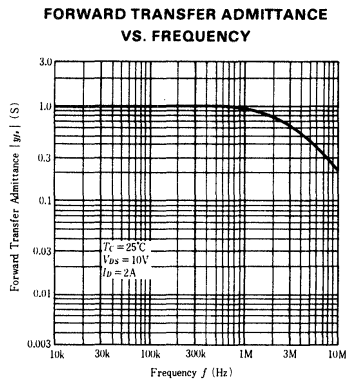
DRAIN - SOURCE VOLTAGE VS. GATE - SOURCE VOLTAGE



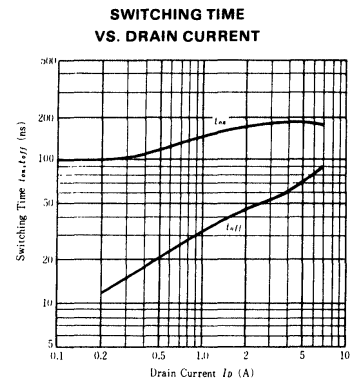
INPUT CAPACITANCE VS GATE SOURCE VOLTAGE



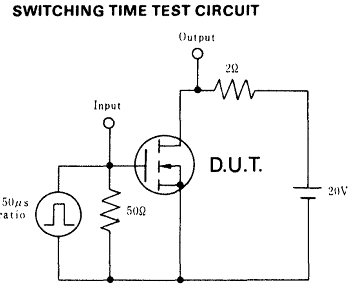
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



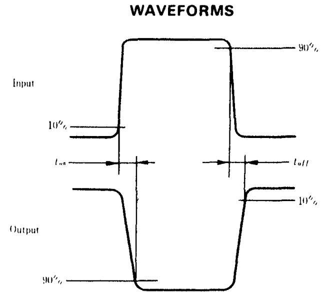
SWITCHING TIME VS. DRAIN CURRENT



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



2SK175, 2SK176

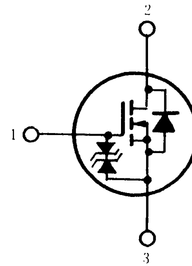
SILICON N-CHANNEL MOS FET

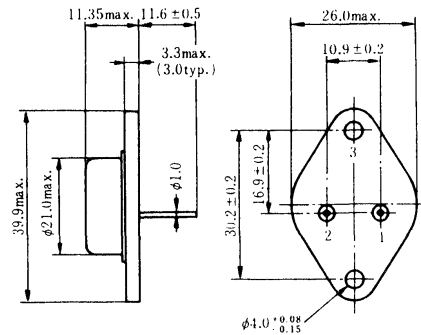
LOW FREQUENCY POWER AMPLIFIER

Complementary pair with 2SJ55, 2SJ56

■ FEATURES

- High Power Gain.
- Excellent Frequency Response.
- High Speed Switching.
- Wide Area of Safe Operation.
- Enhancement-Mode.
- Good Complementary Characteristics.
- Equipped with Gate Protection Diodes.





1. Gate
2. Drain
3. Source (Case)

(Dimensions in mm)

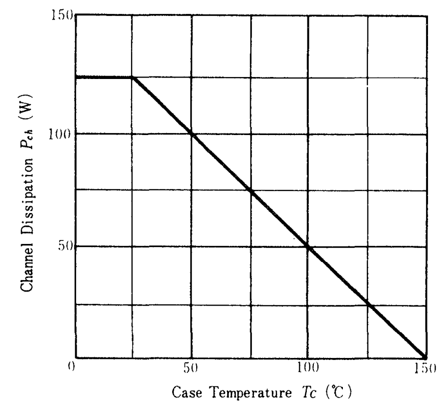
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating		Unit
		2SK175	2SK176	
Drain-Source Voltage	V_{DSX}	180	200	V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current	I_D	8		A
Body-Drain Diode Reverse Drain Current	I_{DR}	8		A
Channel Dissipation	P_{ch}*	125		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 ~ +150		°C

*Value at T_C=25 °C

POWER VS. TEMPERATURE DERATING

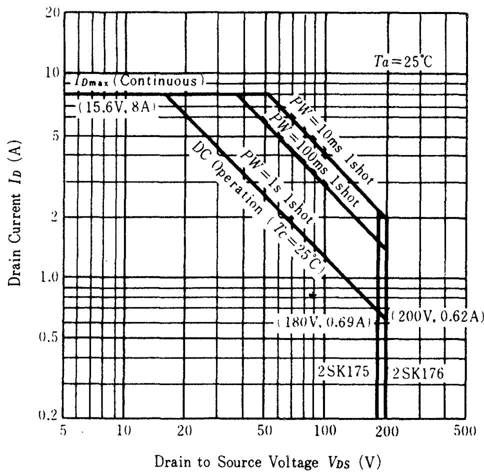


■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

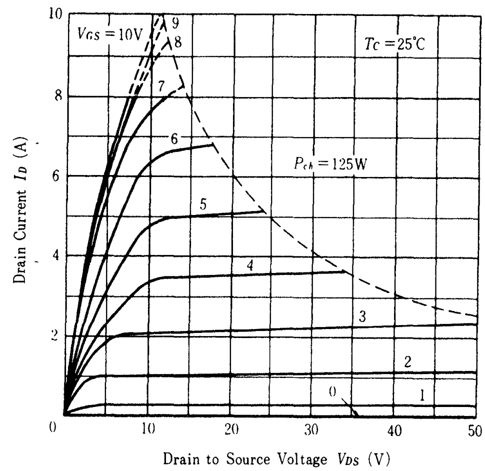
Item		Symbol	Test Condition	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	2SK175	$V_{(BR)DSX}$	I_D=10mA, V_{GS}=−10V	180	—	—	V
	2SK176			200	—	—	V
Gate-Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	—	—	V
Gate-Source Cutoff Voltage		$V_{GS(off)}$	I_D=100mA, V_{DS}=10V	0.15	—	1.45	V
Drain-Source Saturation Voltage		$V_{DS(sat)}$	I_D=8A, V_{GD}=0*	—	—	12	V
Forward Transfer Admittance		$\|y_{fs}\|$	I_D=3A, V_{DS}=10V*	0.7	1.0	1.4	S
Input Capacitance		C_{iss}	V_{GS}=−5V, V_{DS}=10V, f=1MHz	—	800	—	pF
Output Capacitance		C_{oss}		—	600	—	pF
Reverse Transfer Capacitance		C_{rss}		—	15	—	pF
Turn-on Time		t_{on}	V_{DD}=30V, I_D=4A	—	250	—	ns
Turn-off Time		t_{off}		—	90	—	ns

*Pulse Test

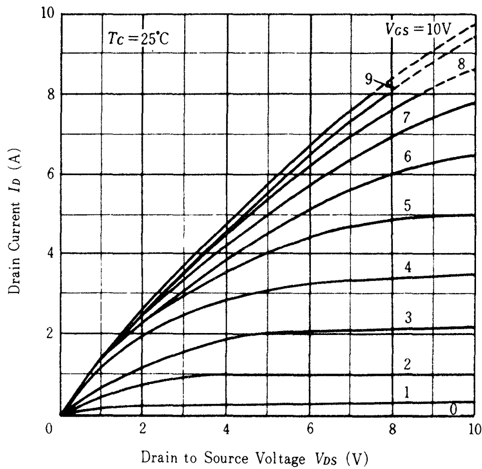
MAXIMUM SAFE OPERATION AREA



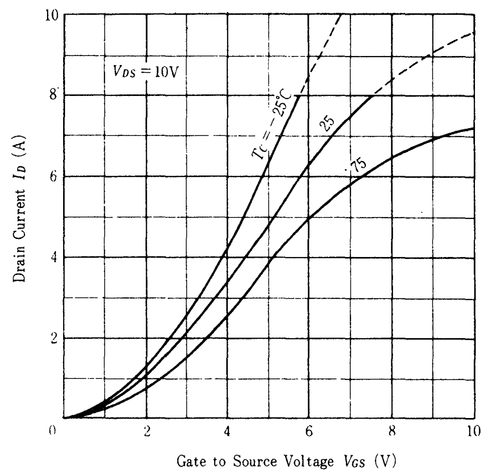
TYPICAL OUTPUT CHARACTERISTICS



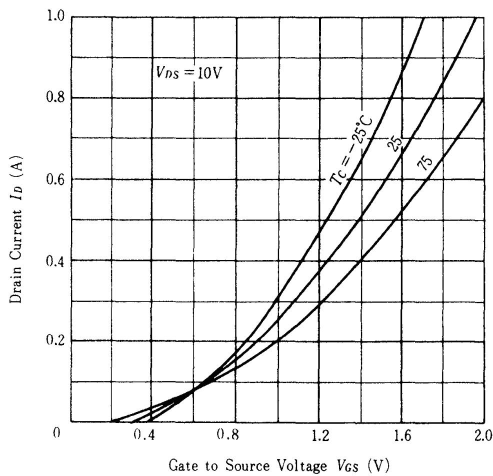
TYPICAL OUTPUT CHARACTERISTICS



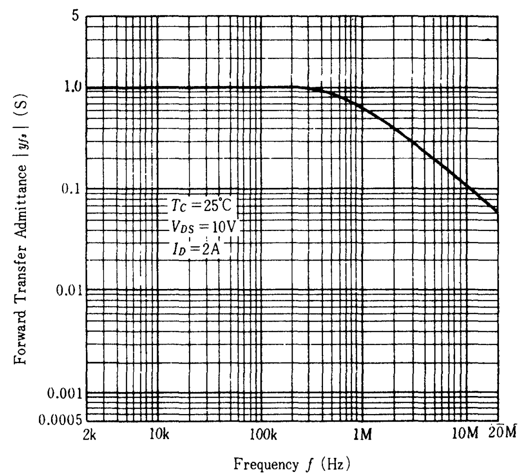
TYPICAL TRANSFER CHARACTERISTICS



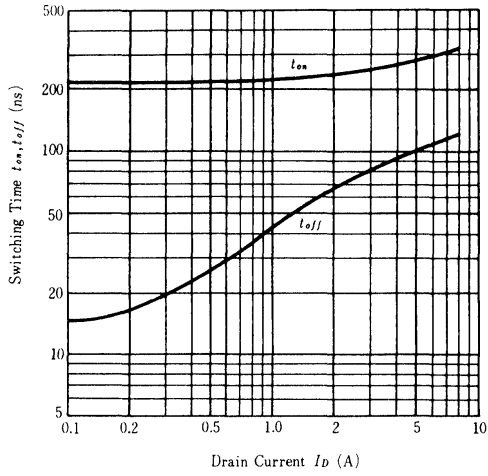
TYPICAL TRANSFER CHARACTERISTICS



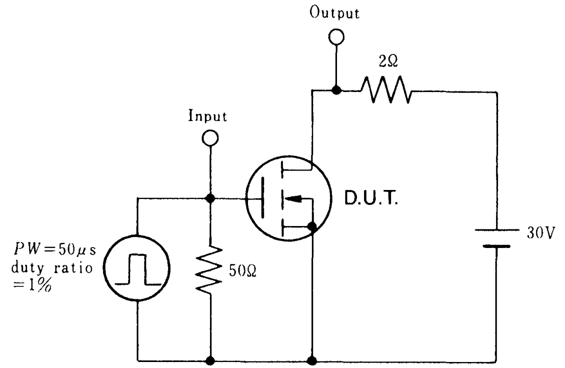
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME VS. DRAIN CURRENT

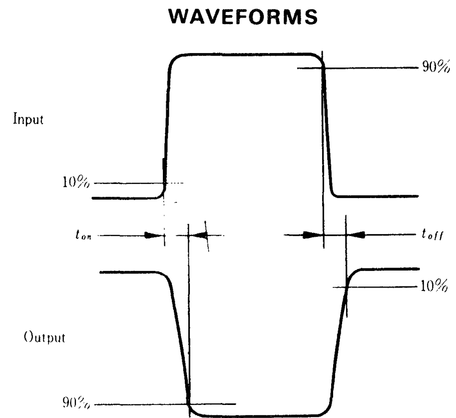


SWITCHING TIME TEST CIRCUIT



RESPONSE WAVEFORM

WAVEFORMS



1.APPLICATION HINTS

1.1 Audio Power Amplifier

1.1.1 Linear Power Amplifier

(1) Design of output stage (Design of power supply voltage V_{DD})

Fig. 1-1 shows an equivalent circuit of the output stage. R_{ON} is a drain-to-source equivalent resistance when the power MOS FET is on, and according to the 2SK134/2SJ49 spec, it is;

$$R_{ON} = \frac{V_{DS(sat)}}{I_D} = \frac{12}{7} = 1.71\Omega$$

The peak current I_p flowing through load $R_L=8\Omega$ at Po=100W is calculated from mean current I,

$$P_O = I^2 R_L$$

$$I_p = \sqrt{2} \cdot I = \sqrt{\frac{2P_o}{R_L}}$$

$$= \sqrt{\frac{200}{8}} = 5\text{ A}$$

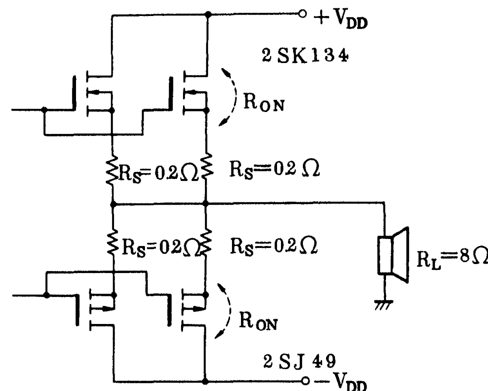


Fig. 1-1 Equivalent Circuit of the Output Stage

Therefore, if the transformer regulation is estimated at 20% and the AC line regulation at ±15%, then the power supply voltage V_{DD} is given as;

$$V_{DD} = 1.2 \times 1.15 \left\{ R_L + \frac{(R_{ON} + R_s)}{2} \right\} I_p$$

$$\fallingdotseq 61.8\text{ V}$$

In Fig. 1-3, the power supply of power stage is common with that of voltage amplifier stage, so the voltage is set at ±65V including the gate-to-source ON voltage at Po=100W.

In the case of D series 2SK343/2SJ99, the R_{ON} value is very small (0.5Ω), the supply voltage required for the same output (100W) is only 57.6V. This enables us to make the transformer capacity and the cooling fin smaller, resulting in cost reduction.

(2) Design of voltage amplifier stage

A power MOS FET can be driven by a low driving power. Fundamentally, only power for charging and discharging the gate-to-source capacitance is needed by the output stage, so that a class B driver stage is not required. The driving power varies with input frequency. At 100W output and 100kHz frequency, it would be very small as follows.

$$Pin = f \cdot Ciss \cdot V_{GS}^2 = 100 \times 10^3 \times 900 \times 10^{-12} \times 6^2 = 3.24\,\text{mW}$$

Therefore, an output stage power MOS FET can be driven directly from a class A predriver (voltage amplifier stage) used in a bipolar transistor amplifier. By eliminating the class B driver, the quantity of components can be reduced, and impairment of the amplifier's performance by the driver itself can be avoided. Moreover, the number of poles in the transfer function (open loop gain vs. frequency characteristics) decreases, and the stagger can easily be increased. Consequently, the stability against oscillation is improved. Transistors for the voltage amplifier stage are required to have a high breakdown voltage, low Cob (collector output capacitance) and high f_T (gain-bandwidth product).

(3) Open loop voltage gain

The transconductance $|y_{fs}|$ of power MOS FETs is as large as 1.0 ∿ 2.5S typ. Yet it is only a fraction of that of bipolar transistors. For example, $|y_{fs}|$ of bipolar transistors at I_C (collector current)= 1.0A, is very large, as follows;

$$|y_{fs}| = \frac{1}{r_e} = \frac{I_E}{KT/q} = \frac{1\,A}{26\,mV} \fallingdotseq 38\,S$$

where r_e: Emitter equivalent resistance
K: Boltzmann constant
T: Absolute temperature
q: Electron charge
I_E: Emitter bias current

When the power device is used in the source follower (In bipolar transistor circuit; it's called emitter follower), the relationship between input and output is;

$$\frac{\text{output}}{\text{input}} \doteq \frac{R_L}{R_L+1/|y_{fs}|}$$

(See Fig. 1-2)

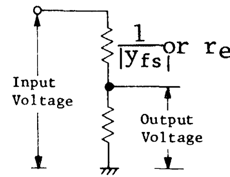


Fig. 1-2 Source Follower Input & Output

Only the nonlinear component of this equation, $1/|y_{fs}|$, causes distortion, so that a larger $|y_{fs}|$ is of lower distortion. In other words, since a power MOS FET amplifier has a distortion about 20dB larger than a bipolar transistor amplifier, it is necessary to design for larger open loop gain and larger negative feedback than in a bipolar transistor circuit.

(4) Considerations for parasitic oscillation

Because power MOS FETs have excellent high-frequency characteristics, they are liable to cause oscillation, even in a simple circuit.

For an analysis of stability in a source follower circuit, see paragraph 5.9 (page 47). Here, we would like to show some precautions in fabrication.

- Minimize the wiring between the printed circuit board and the power MOS FETs. Direct connection is recommended.
- Provide one-point grounding for the amplifier printed circuit, power supply, and speaker terminals. Make the wiring of power supply line and ground line as big as possible.
- The output coupling coil L has the effect of reducing distortion in the high frequency range. It also prevents oscillation which might occur when the output is loaded by capacitance.
  Its value should be determined experimentally.
- Printed circuit layout should flow topographically from input to output.

(5) Line up

Table 1-1 Line-up of Devices in Audio Amplifier

Output Power		Input Stage			Driver Stage				Output Stage	
			Bipolar		FET (V_{DSX})		Bipolar (V_{CEO})		FET (V_{DSX})	
Single Pushpull	Parallel Pushpull	FET	NPN	PNP	N Channel	P Channel	NPN	PNP	N Channel	P Channel
50~60	—	2SK190 2SK186	2SC1775 2SC2855	2SA872 2SA1190	2SK213 (140V)	2SJ76 (-140V)	2SD756 (120V)	2SB716 (-120V)	2SK133 (120V)	2SJ48 (-120V)
60~80	100~120				2SK214 (160V)	2SJ77 (-160V)	2SD756A (140V)	2SB716A (-140V)	2SK134 (140V) 2SK413 (140V)	2SJ49 (-140V) 2SJ118 (-140V)
—	120~140	—			2SK215 (180V)	2SJ78 (-180V)	2SD668A (160V)	2SB648A (-160V)	2SK135 (160V) 2SK414 (160V)	2SJ50 (-160V) 2SJ119 (-160V)
80~100	—				2SK216 (200V)	2SJ79 (-200V)	2SD758 (200V)	2SB718 (-200V)	2SK175 (180V)	2SJ55 (-180V)
—	140~200	—	2SC1775A 2SC2856	2SA872A 2SA1191	—	—			2SK400 (200V) 2SK176 (200V)	2SJ114 (-200V) 2SJ56 (-200V)

Underline is D Series (Drain Case Type)

(6) Application Circuit

● 100W Output THD≒0.01%, f=100kHz

Q_1, Q_2 : 2SA872
Q_3 : 2SB716A
Q_4, Q_5 : 2SD756A
Q_6, Q_7 : 2SK134
Q_8, Q_9 : 2SJ49

Unit R : Ω
C : F
L : H

Fig. 1-3 P_O=100W Power Amp. Circuit Diagram

Fig. 1-4 Total Harmonic Distortion vs. Output Characteristics

Fig. 1-5 Power Band Width

● 100W Output THD≒0.01%, f=50kHz
(All FET DC Amplifier)

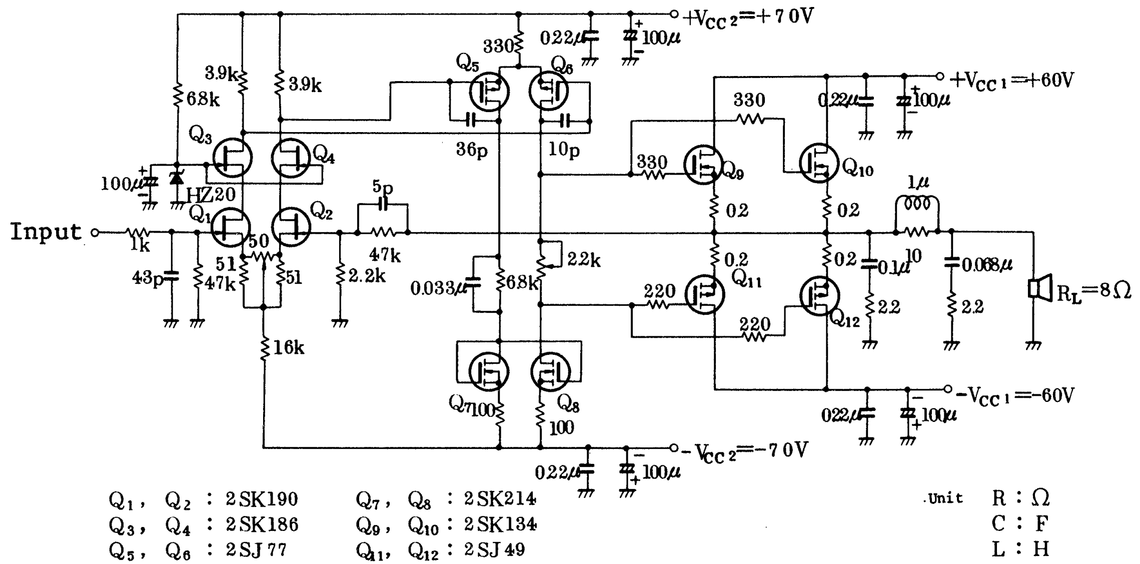


Fig. 1-6 Po=100W All FET Power Amp. Circuit Diagram

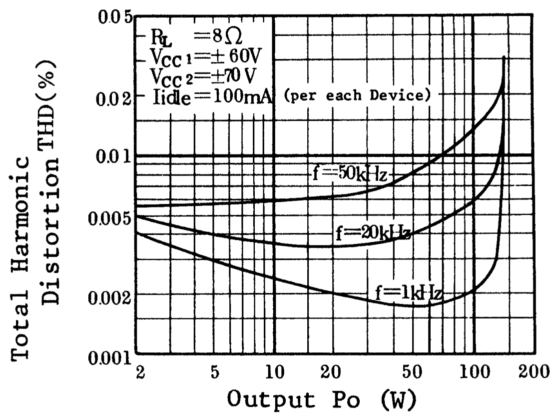


Fig. 1-7 Total Harmonic Distortion vs. Output Characteristics

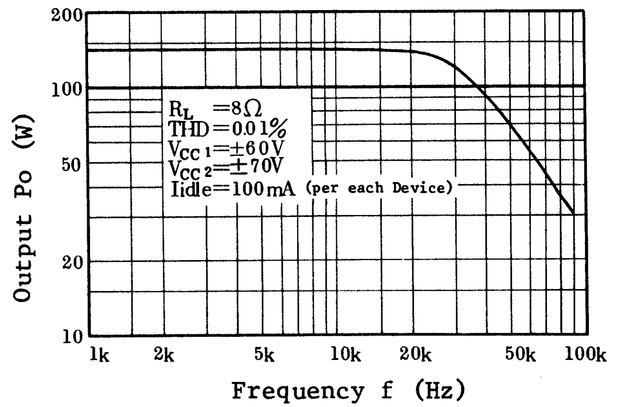


Fig. 1-8 Power Band Width